The Next Generation in Analog and RFIC Design
“The complexity of today’s new technologies renders traditional design methods inadequate in terms of accuracy, efficiency and cost. An entirely new EDA approach is required in order to ensure complete design closure between IC, package, module, and PCB design phases. The Analog Office design system provides the ability to achieve optimum RF closure through a unified data model and single design environment encompassing all of the design domains.”

James Spoto, President and CEO, AWR
Analog Office 2004
The Next Generation in Analog and RFIC Design

Applied Wave Research, Inc. (AWR™) has established itself as a leading worldwide provider of high-frequency electronic design automation (EDA) software. The company has developed a revolutionary, future-facing product architecture and open system platform that embodies years of knowledge and expertise in RF, microwave, and millimeter wave design applications and delivers an unprecedented level of design automation and productivity improvement not offered in any other design system on the market today. AWR has introduced some of the most exciting and compelling high-frequency design tools in the industry, while completely resetting expectations on how fast a software developer can react to the needs of its customers. As a result of its industry leading product innovation and customer responsiveness, AWR has established a loyal worldwide customer base that continues to expand rapidly.

EDA has evolved over the past 20 years as isolated activities for each phase of a design. Legacy systems have separated the electrical design/analysis from the physical implementation domains at both the IC and package/module and printed circuit board (PCB) levels. EDA vendors have developed closed methodologies and tool sets for different design phases, requiring manual hand-offs and multiple iteration loops that result in costly errors and delays. The complexity of today’s new semiconductor process technologies, as well as module implementation technologies, however, renders traditional design methods inadequate in terms of accuracy, efficiency, and cost.

The high-frequency circuit impairments in today’s complex analog and RF ICs, such as: compression, noise, distortion, and phase noise, as well as the physical parasitics such as interconnect impedance and coupling, are forcing the need to obtain complete “RF closure” between the RFIC’s system and circuit, electrical and physical, and design and test activities before commitment to costly IC implementation.

AWR Design Environment
Built on an advanced software architecture, the unique core technology in the AWR Design Environment™ is a modern object-oriented data model that is inherently open and flexible compared to legacy design tools. The AWR Design Environment elevates the product development process by allowing the entire engineering team to effortlessly integrate Analog Office circuit designs into one platform with Visual System Simulator™ (VSS) for system design and TestWave™ for simulation with test and measurement equipment, providing an accurate understanding of the impact of today’s complex...
“AWR has a remarkable team and some of the most innovative and compelling technology I have seen to address the unique requirements of high-performance analog and RFIC design. In addition to enhancing productivity, I believe this unified system provides the best usability in the industry.”

James Solomon
Founder
Cadence Design Systems

modulated RF signals and "real world" circuit performance. The result is a truly revolutionary design approach that enables interactive tradeoffs between system requirements and circuit implementation.

AWR’s open software architecture and industry-standard application programming interface give customers easy access into the underlying data structures, allowing seamless integration with other best-in-class tools and design environments. This protects customers’ investment in models and simulators, lowers their cost of support, and enables easy customization of specific flow requirements.

Analog Office Design Suite

The Analog Office design suite is the first complete IC design system in over 10 years that is specifically architected and optimized from the ground up for next generation analog and RFIC designs. Much more than a point tool, the Analog Office integrated solution boasts an industry-first, concurrent interconnect-driven and RF-aware design methodology that delivers unprecedented ease-of-use, interactivity, and openness.

Analog Office software was created by the experienced development team that originally developed Cadence’s Analog Artist design environment and leverages years of cutting edge design experience.

The Analog Office design system provides an entirely new approach that achieves optimum RF closure through a unified data model and design environment encompassing all of the design domains. The data model is high-frequency aware, permitting accurate extraction and modeling of all design elements, including active and passive devices, as well as interconnects, at high-frequency. The new solution is built on AWR’s open, standard-based software platform, enabling easy integration of the most capable, best-in-class tools to: capture, synthesize, simulate, optimize, layout, extract, and verify designs from system to final tape-out. The Analog Office design suite is fully integrated into existing digital and mixed signal IC design flows from Cadence and Synopsys, and enables analog and RFIC design engineers to significantly shorten their development cycles and speed wireless products to market.
Complete Front-to-Back Analog and RFIC Design System

The Analog Office unified design environment fully interacts with a comprehensive and powerful set of integrated tools for top-down and front-to-back analog and RFIC design. The toolset spans the entire IC design flow, from system-level to circuit-level design and verification, and includes:

**Easy-to-use graphical user interface supporting**
- System- and circuit-level design methodologies
- Electrical and physical design, schematic capture, simulation/analysis, and layout and verification
- Frequency- and time-domain simulation and analysis
- Links from design to test

**Integrated waveform display and analysis capabilities supporting complex RF measurements**
- Hundreds of pre-built measurements
- Parametric tuning
- Noise analysis
- Sweep parameter analysis
- Multiple test benches with multiple simulators
- Statistical analysis
- Optimization

**Support for different types of simulation**
- System simulation with Visual System Simulator
- Time-domain simulation with Synopsys’ HSPICE™
- Frequency-domain simulation with AWR’s harmonic balance simulator
- Electromagnetic (EM) simulation with AWR’s EMSight™

**Open platform for 3rd party tool integration**
- SPICE socket for 3rd party SPICE-based circuit simulators
- EM Socket™ for 3rd party EM simulators

**Powerful and easy-to-use physical design suite**
- Fully interactive layout editor supporting polygon editing and parameterized layout cells
- Automated device-level placement and interconnect routing
- Integrated and interactive design rule checker (DRC)
- Three dimensional (3D) full field solver-based extraction with industry gold standard, high-speed extraction technology from OEA International

Coupled with industry-leading semiconductor foundry design kits for silicon germanium (SiGe) and RF complementary metal-oxide semiconductor (CMOS) processes, as well as gallium arsenide (GaAs), Analog Office software is the first completely new system in over a decade that delivers concept-to-verification design capabilities.

“Using Analog Office design software, we are able to analyze our advanced RF front-end circuits in greater detail than ever before, and in the same environment we are able to see the system ramifications of a circuit-level change. This is extremely powerful in RF system design.”

Kartik Sridharan
Vice President of Engineering
Ashvattha Semiconductor, Inc.
Concurrent Interconnect-Driven/RF-Aware Design Methodology

Integral to the Analog Office software is an industry-first interconnect-driven/RF-aware design methodology built around AWR’s iNet technology. Similar to a timing-driven or wire-driven digital design methodology, the interconnect-driven/RF-aware methodology focuses on accurate RF interconnect modeling and analysis throughout the entire RFIC design process to reduce or eliminate design iterations, shorten the design cycle, and ensure first-time design success. Unlike existing net constructs built on a “digital-centric” data model, the Analog Office iNet technology is based on an RF-accurate net model with multiple levels of abstraction. Models for short-circuit, lumped, resistance-inductance-capacitance (RLC), distributed RLCK (including coupling inductance), fully distributed transmission line, or full 3D EM elements, use a single environment and data model. iNet technology provides concurrent and real-time physical modeling of RF interconnects while the layout is in progress, eliminating the need for a serial post-layout connectivity extraction step. Simulation and analysis can be invoked immediately to verify the performance of the design as soon as the critical nets are laid out, without waiting for the rest of the circuit to be completed, ensuring early and complete RF design closure.

Measurement-Driven Paradigm

Analog Office 2004 design suite has pioneered a new, yet more natural, paradigm for high-frequency design. In traditional EDA systems, users must undergo multiple design setup steps to obtain a particular analysis result from a selected simulator, necessitating the generation of many data files. In the Analog Office product, however, users simply set up multiple test benches and analysis measurements ahead of time (similar to a specification sheet) and then set up the parameters for the designs. As soon as the simulation is started, the system automatically selects the “right” simulator for the particular analysis, extracts the “right” models for the design elements, runs the simulator(s), obtains the results and processes them into requested measurements, and presents the results in multiple graphs and tables. In the same environment, users can dynamically “tune” the design across a set of parameters, test benches, and simulators very quickly and efficiently. The Analog Office measurement-driven paradigm significantly improves the productivity of the RF design process.
Powerful Analog and RF Simulation Technologies

The focus of any EDA solution is limited by the power of its simulation technology, and Analog Office design suite pushes the standard industry limits to solve larger and more complex problems quickly and efficiently. AWR provides one of the industry’s fastest harmonic balance simulators, which performs 10 to 1000 times faster than similar products for most problems. This improved simulation performance is coupled with proprietary convergence algorithms that extend the capacity of the simulator to handle large and highly nonlinear circuits. The superior speed and capacity of the simulator can also open designs up to more rigorous statistical modeling and yield analysis, which now becomes practical on circuits that may have consumed too much simulation time in the past.

The Analog Office time-domain simulator provides an important complement to its harmonic balance simulator and can solve unique problems such as those found in phase lock loops (PLLs) or oscillators during start-up conditions. Analog Office software is the first solution to include an optional time-domain engine to augment its harmonic balance, Voltera, and EM simulators. Much more than just another SPICE simulator, AWR’s time-domain engine is integrated with Synopsys’ golden standard HSPICE®, providing the fastest, most accurate, highest capacity simulations, as well as hundreds of foundry-proven built-in device models for most commercial IC foundries.

Open, Standard-Based Process Design Kits Supporting Popular Silicon Foundries

The integrity of the electrical and physical model data is often a contentious issue between foundry customers, foundries, and EDA vendors. Neither an EDA company nor a foundry can deliver an optimal PDK in isolation. AWR, initially driven by customer demand, has established close partnerships with leading RFIC foundries to develop and deliver validated PDKs that include integrated electrical models with schematic symbols and simulation models, parameterized layout cells, and DRC rules files, enabling an efficient and error-free RFIC design flow. AWR is engaged with all the major semiconductor foundries worldwide to develop foundry-specific libraries or design kits targeting SiGe, BiCMOS, and RF CMOS processes. AWR currently provides PDKs for TSMC, Jazz Semiconductor, and IBM foundry processes.

“Finisar takes great pride in providing leading-edge products that exemplify our commitment to engineering excellence, product reliability, and customer value. The Analog Office open, integrated platform and unique RF-aware design methodology provide our engineers with the accurate RF modeling and analysis needed to design products that meet our exacting standards.”

James Douma
Transponder Engineering Manager
Finisar Corporation
AWR is also actively working for the standardization of custom design kit data as the founding member of the Openkit (OK) Initiative and continues to participate and contribute on the technical subcommittees for the Initiative. Accellera, the electronics industry organization focused on language-based electronic design standards, has tasked the subcommittee, which includes representatives from semiconductor, EDA, foundry, and library/IP companies, with defining standard formats that represent information related to process technology, design tool requirements, and IC design requirements.

End users, commercial foundries, and EDA vendors can all benefit from the reduced support effort, higher customer satisfaction, and shorter design cycles that result from integrated foundry libraries and standardized formats.

**Physical Layout with Automatic Placement and Routing, Integrated DRC and Embedded 3D Extractor**

Analog Office design suite provides IC designers with a complete physical design system to fully implement their analog and RF IC designs within a single environment, eliminating the need for switching between multiple environments and databases.

The Analog Office package offers a completely interactive custom layout tool with integrated device-level, auto-placement, and auto-routing features to speed up the creation of analog and RF circuit blocks and chips. An integrated DRC ensures the physical layout being created always meets the process design rules, resulting in a correct-by-design, error-free layout. The layout editor is directly connected to the EM socket, providing “on-the-fly” EM extraction and modeling of arbitrary layout structures and complex spiral inductors. At every step during the physical design process, AWR’s iNet technology continuously updates in real time the underlying interconnect data model, and after each interconnect is “implemented” or laid out, concurrent simulation and analysis can be immediately invoked on the schematic or layout to verify the performance of the overall design without waiting for the final layout of the whole design to be completed.
To ensure proper modeling of inductance coupling between nets in gigahertz physical layout, the Analog Office design system also integrates the Cheetah 3D field solver, the core interconnect extraction technology from OEA International's NET-AN™ 3D critical multi-net field simulator. The selected net or nets are automatically extracted and modeled as distributed RLCK for fast and accurate simulation. This level of interconnect modeling complements other modeling levels that are managed by iNet technology, such as lumped RLCs and fully distributed transmission lines, thus extending the designer's range of design trade-off flexibility between simulation run-time performance and modeling accuracy.

Seamless Integration with Cadence's Mixed-Signal IC Design Flow
Analog Office design suite can be used to design the entire analog or RF IC from system-level modeling and simulation through to final layout and tape-out. The Analog Office suite of tools generates the necessary industry-standard files, such as layout vs. schematic (LVS) netlist and GDSII, to interface to a final verification flow based on industry-popular IC physical verification tools from Mentor Graphics, Synopsys, and Cadence.

Analog Office software can also be used to design complete RF blocks as part of a large mixed-signal system-on-chip (SoC). In this flow, AWR provides complete, bi-directional data transport capabilities to and from standard industry mixed-signal IC design flows, including Cadence’s Design Framework II (DFII)-based analog/mixed-signal flow, for full chip assembly, physical verification, chip finishing, and tape-out. The data transport solution currently supports the Cadence Virtuoso® custom design platform, including the Composer schematic editor, the Analog Design Environment (ADE) (formerly Analog Artist), and the Virtuoso layout editor. The solution transfers full Composer schematic data, such as: schematic symbol graphics, interconnect wires, connectivity information, component properties, schematic and global equations, and a host of other ADE-specific design data. The data transport solution can also transfer layout data between Analog Office and the Virtuoso layout environment while maintaining parameterized cell (Pcell) information and mapping. An LVS netlist can be generated from Analog Office software for final verification in the Cadence design environment.

AWR is actively working with OpenAccess to ensure a smooth path between Analog Office design system and an OpenAccess-based Cadence design flow. The resulting integrated flow is similar to the current Analog Office and Cadence Design Framework II integrated flow, except that OpenAccess is now the common database.

“Sophisticated RF tools and flow are needed to complete large, complex, mixed-signal SoCs and to ensure the design will work before it gets into fabrication. AWR products are specifically architected and optimized to extend the range of possible analog and RF design solutions to meet this challenge.”

Alan Su
ITRI Technical Manager of IP Technology and Design Automation
Nankang Taiwan SoC Design Park
Target Applications

The Analog Office design suite can be used to design many high-frequency RFICs that are at the heart of next-generation wireless devices. These ICs, which operate at the 2.4, 5.8, and higher gigahertz frequency spectrum, drive a wide range of wireless applications such as wireless local area networks (LANs), 802.11a/b/g, and 2.5G and 3G wireless handsets and base stations, as well as emerging wireless broadband applications such as Wi-MAX and ultra wideband (UWB). High-speed networking applications, such as electro-optical transceivers and switches, as well as network access applications such as home gateway boxes, xDSLs, and cable modems also employ many analog ICs at the front end to transmit and receive high-speed signals.

Analog Office software can also be used to design high-precision and high-performance analog ICs such as amplifiers (low noise, differential, logarithmic, etc.), mixers, and modulators and demodulators, as well as high-speed digital circuits such as clock-data recovery circuits (CDRs), PLLs, and voltage-controlled oscillators (VCOs).
"Analog Office is the first completely new IC design system in over a decade. Unlike legacy systems that are built on a digital-centric foundation, Analog Office was crafted from the ground up to address the new challenges in gigahertz electronic product development."

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Call to discuss your specific requirements, arrange a demonstration, or to receive an evaluation CD.

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